

← CHANNEL LENGTH →

↑
100

FIGURE 1A

Diagram illustrating a perspective view of a channel 102. The channel is defined by side walls 128 and a bottom surface 140. It features two vertical dividers 130A and 130B, which partition the channel into three sections. The width of the channel is labeled 'w', and the height is labeled 'h'. The channel length is indicated by a double-headed arrow at the bottom, and the channel width is indicated by a double-headed arrow on the right side.

FIGURE 1B

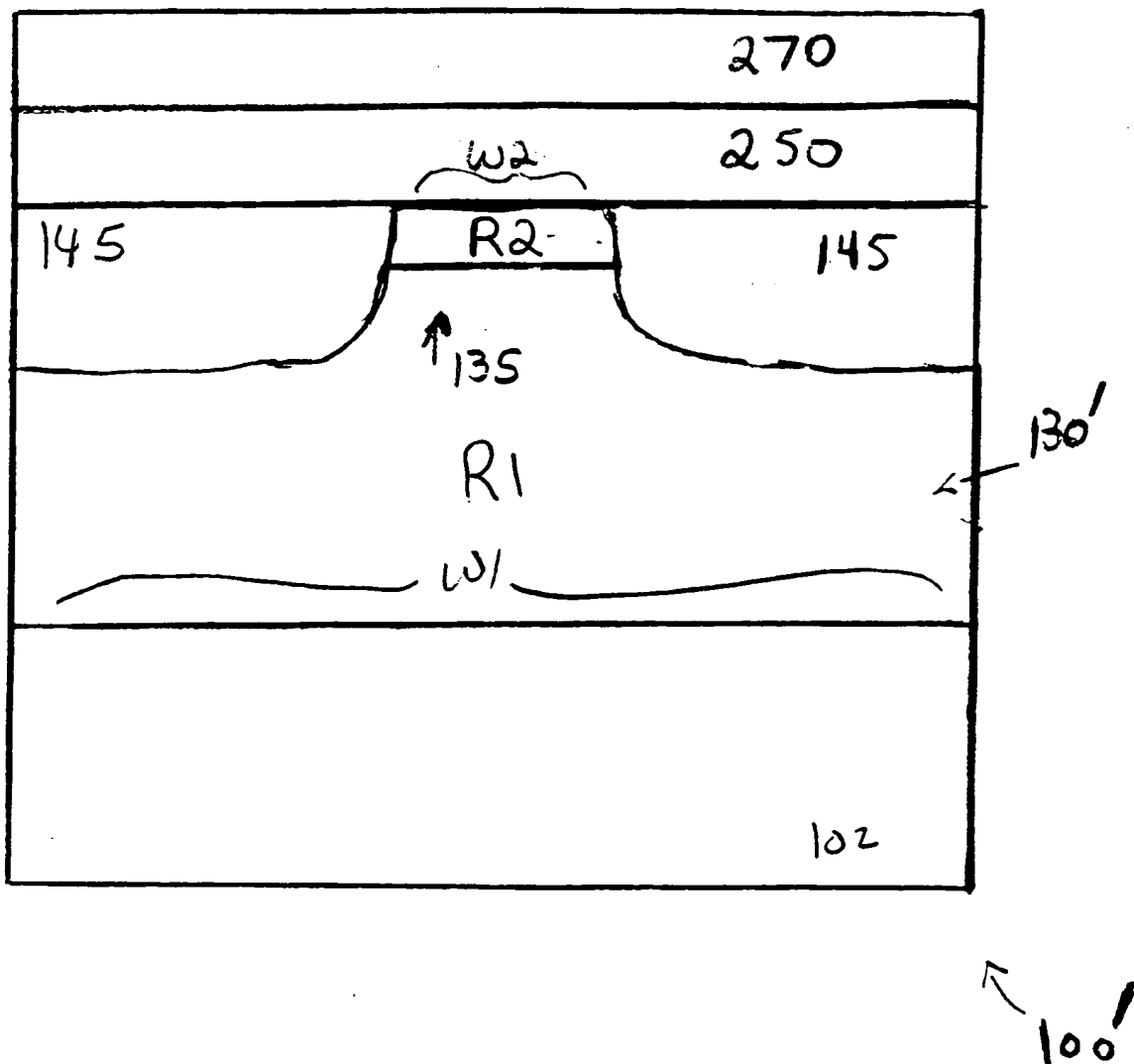


FIGURE 1E

180

270

250

280

132

R_1

128S

128

130A

140

130B

R_2

132

128S

128

106

102

100

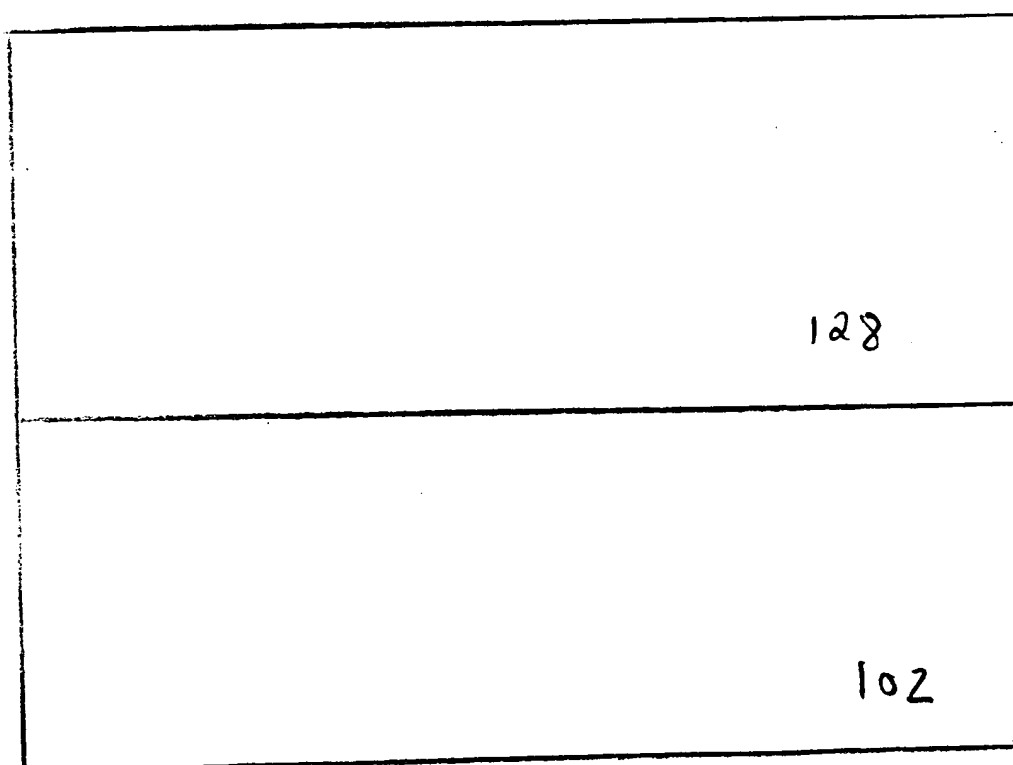
FIGURE 1 F

Hand-drawn schematic diagram of a multi-layer PCB layout. The diagram shows a top layer with dimensions 180, 270, and 250. Below this is a central area with two vertical columns of components labeled R1, R2, and R3. The left column is grouped as 130A and the right as 130B. Dimensions 132, 128S, 128, and 140 are indicated. A bottom layer is labeled 102, and a central horizontal dimension is 106.

100

FIGURE 1G

0900348-072000



↑
200A

FIGURE 2A

A hand-drawn diagram of a three-story building with two wings. The left wing is labeled '128' on the ground floor and '1285' on the second floor. The right wing is labeled '128' on the ground floor and '1285' on the second floor. A central section is labeled '106' on the ground floor and '170' on the second floor. A large rectangular area at the bottom is labeled '102'.

↑
2003

FIGURE 2B

FIGURE 2C

0560318 07P00

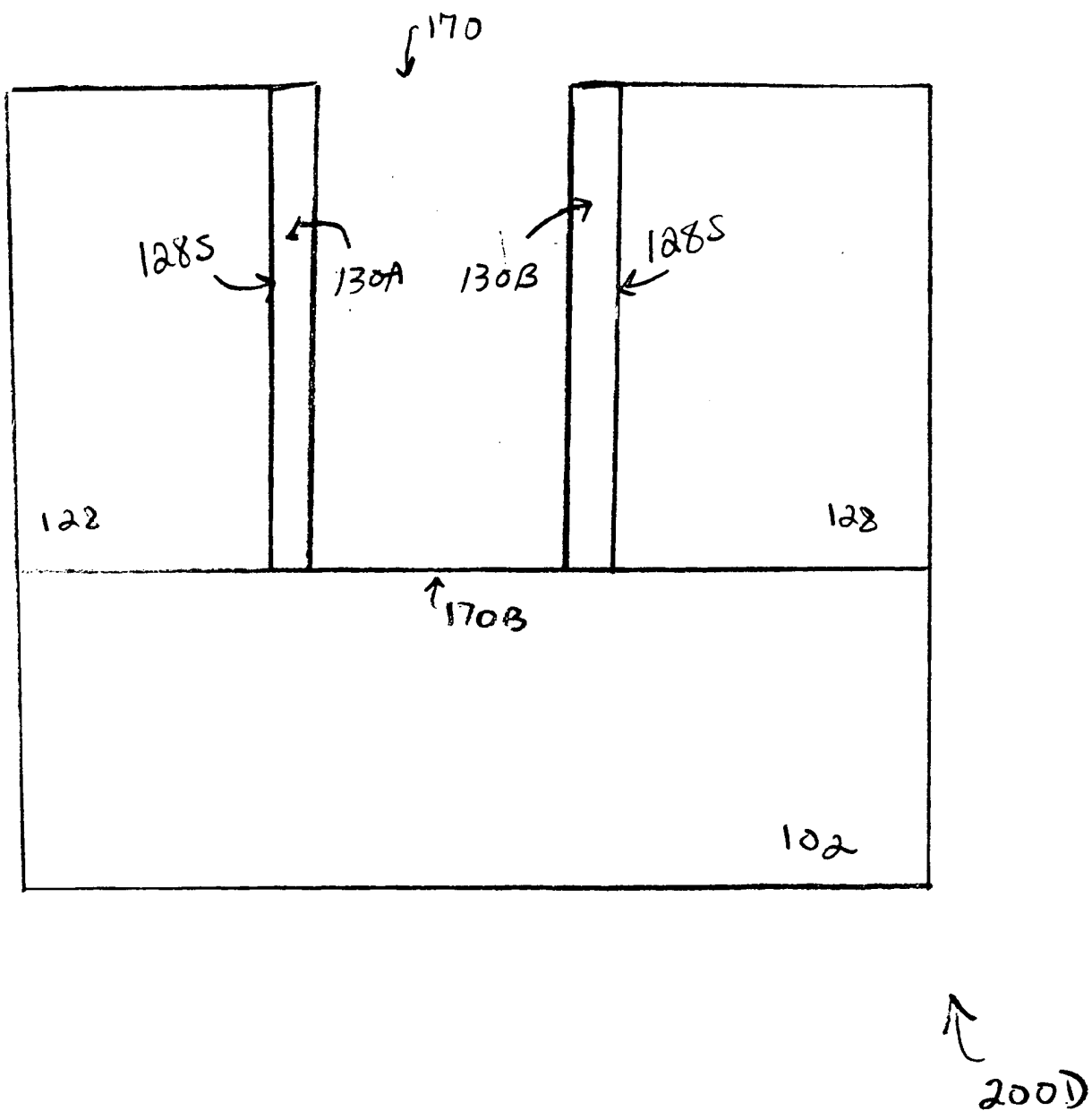


FIGURE 2D

Hand-drawn schematic diagram of a multi-layer PCB layout. The diagram shows a central rectangular area labeled '140' with two vertical strips on either side, labeled '130A' and '130B'. The top and bottom edges of the central area are labeled '140'. The left and right edges of the vertical strips are labeled '128'. The bottom edge of the entire assembly is labeled '102'.

FIGURE 2E

A hand-drawn schematic diagram of a 2D grid. The grid is divided into several regions by vertical and horizontal lines. The top row contains two vertical strips labeled R_1 and R_2 . Above R_1 is a label $130A$ with an arrow pointing left. Above R_2 is a label $130B$ with an arrow pointing right. Above both R_1 and R_2 are labels 132 with arrows pointing down. The bottom row contains a large rectangular area labeled 102 . The left and right sides of the grid are labeled 128 . The central area between the vertical strips is labeled 140 .

↑
200F

FIGURE 2F

132

132

130A

130B

128

128

140

102

FIGURE 26

The diagram illustrates a 140-bit data structure. It is divided into three main sections: a left 132-bit segment, a central 140-bit segment, and a right 132-bit segment. The left 132-bit segment is further divided into a top 132-bit sub-segment (labeled 132) and a bottom 128-bit sub-segment (labeled 128). The right 132-bit segment is similarly divided into a top 132-bit sub-segment (labeled 132) and a bottom 128-bit sub-segment (labeled 128). The central 140-bit segment is labeled 140. The top 132-bit sub-segments are labeled 132A and 132B. The bottom 128-bit sub-segments are labeled 128A and 128B. The labels 132A, 132B, 128A, and 128B are placed next to their respective sub-segments. The labels 132, 140, and 128 are placed next to their respective main segments. The labels 132A and 132B are also placed next to their respective sub-segments. The labels 128A and 128B are also placed next to their respective sub-segments. The labels 132, 140, and 128 are also placed next to their respective main segments. The labels 132A and 132B are also placed next to their respective sub-segments. The labels 128A and 128B are also placed next to their respective sub-segments.

FIGURE 2H

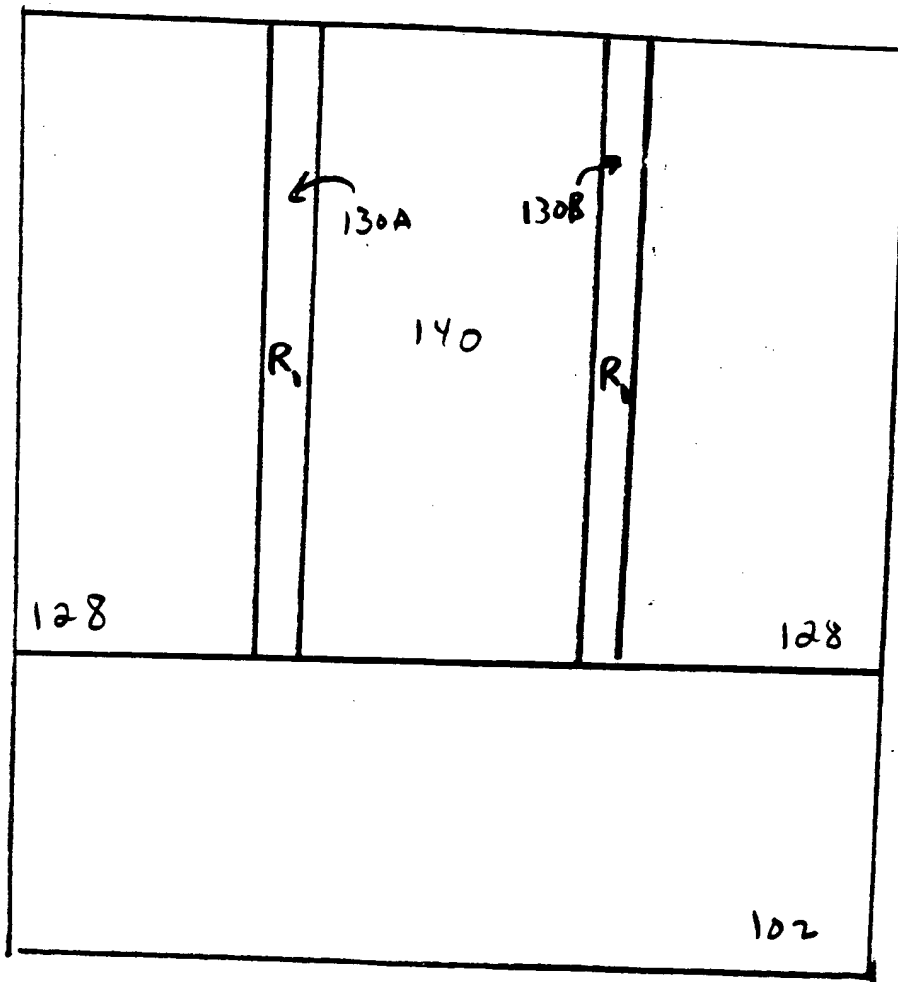
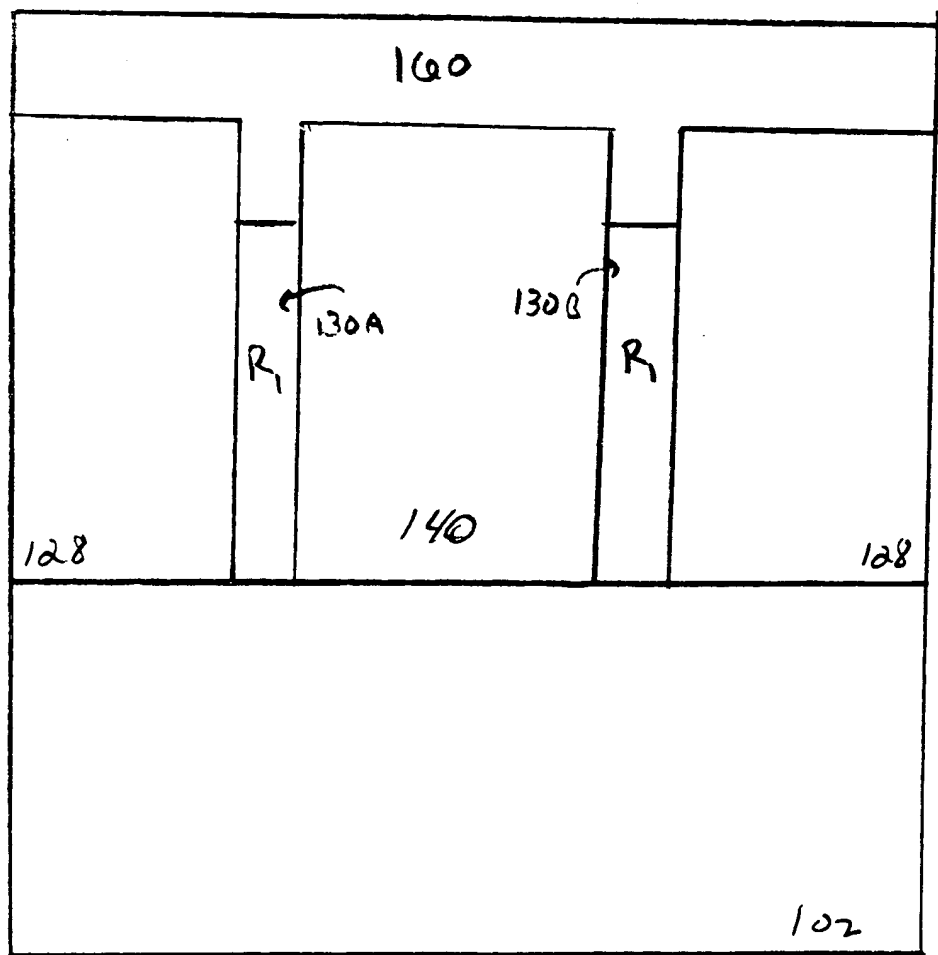


FIGURE 2A

[illegible]

FIGURE 2B'



200C'

FIGURE 2C'

The diagram illustrates a cross-sectional view of a semiconductor device. A central rectangular region is labeled 140. On either side of this central region are two identical vertical structures. Each structure consists of a lower rectangular region labeled R_1 and an upper rectangular region labeled R_2 . A bracket on the left side of the R_1 region is labeled 130A, and a bracket on the right side of the R_1 region is labeled 130B. Above each R_2 region, there is a label 132 with a downward-pointing arrow. A label 160 is placed between the R_1 and R_2 regions of each structure, with an arrow pointing to the boundary between them. The bottom-left corner of the entire structure is labeled 128, and the bottom-right corner is labeled 128. The bottom edge of the entire structure is labeled 102.

200 D'

FIGURE 2D'

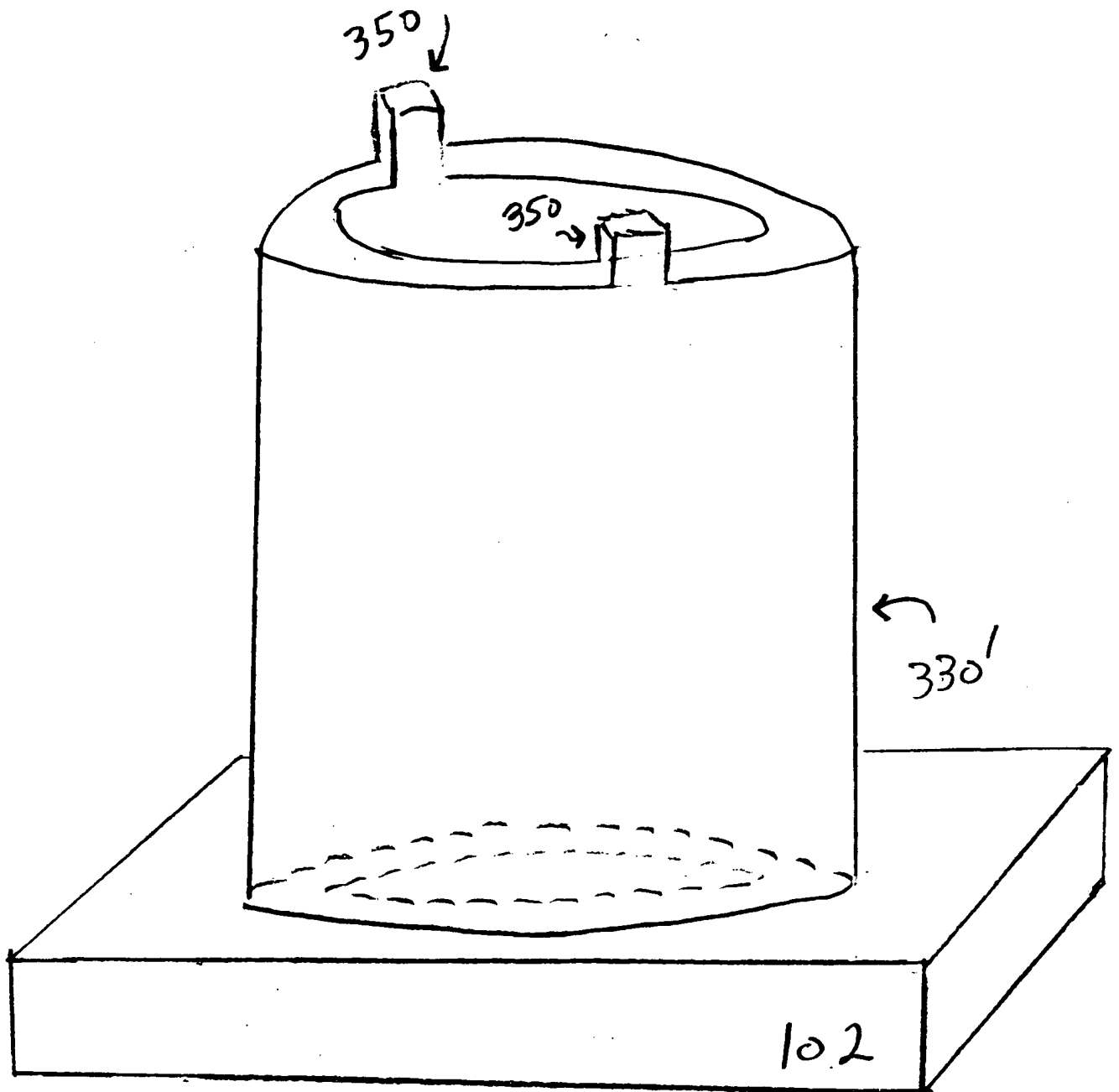


FIGURE 3B

FIGURE 4A

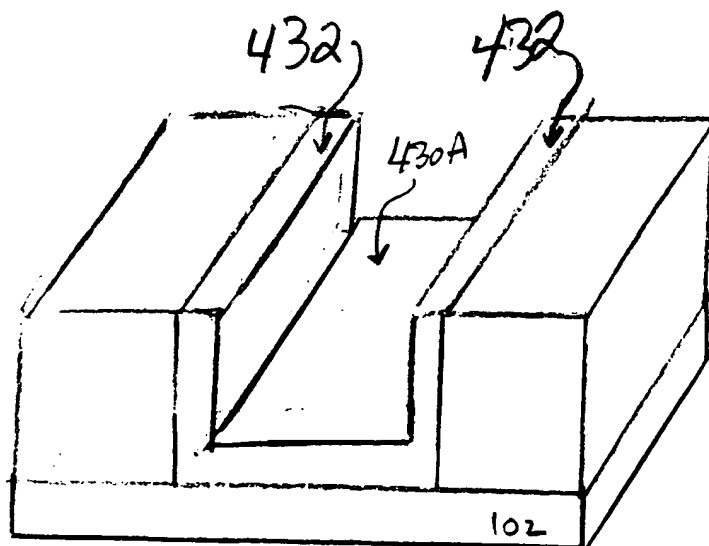


FIGURE 4B

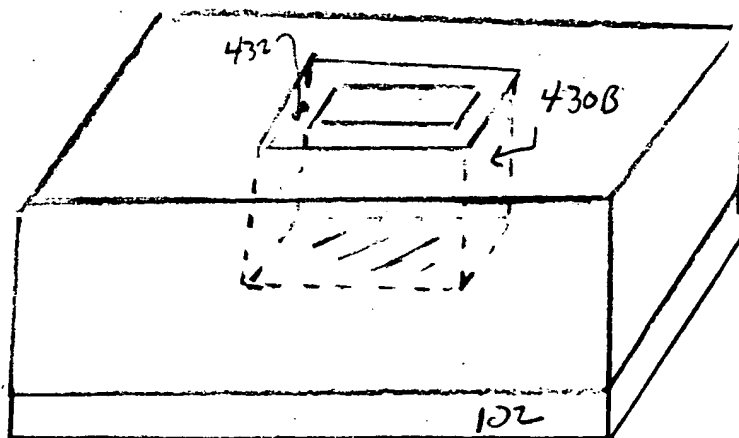
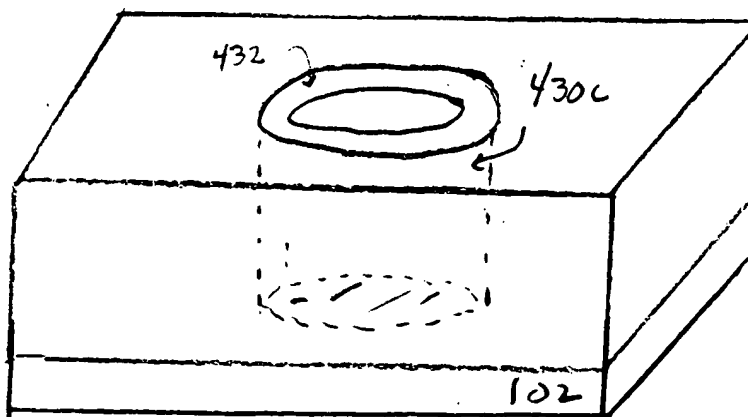


FIGURE 4C



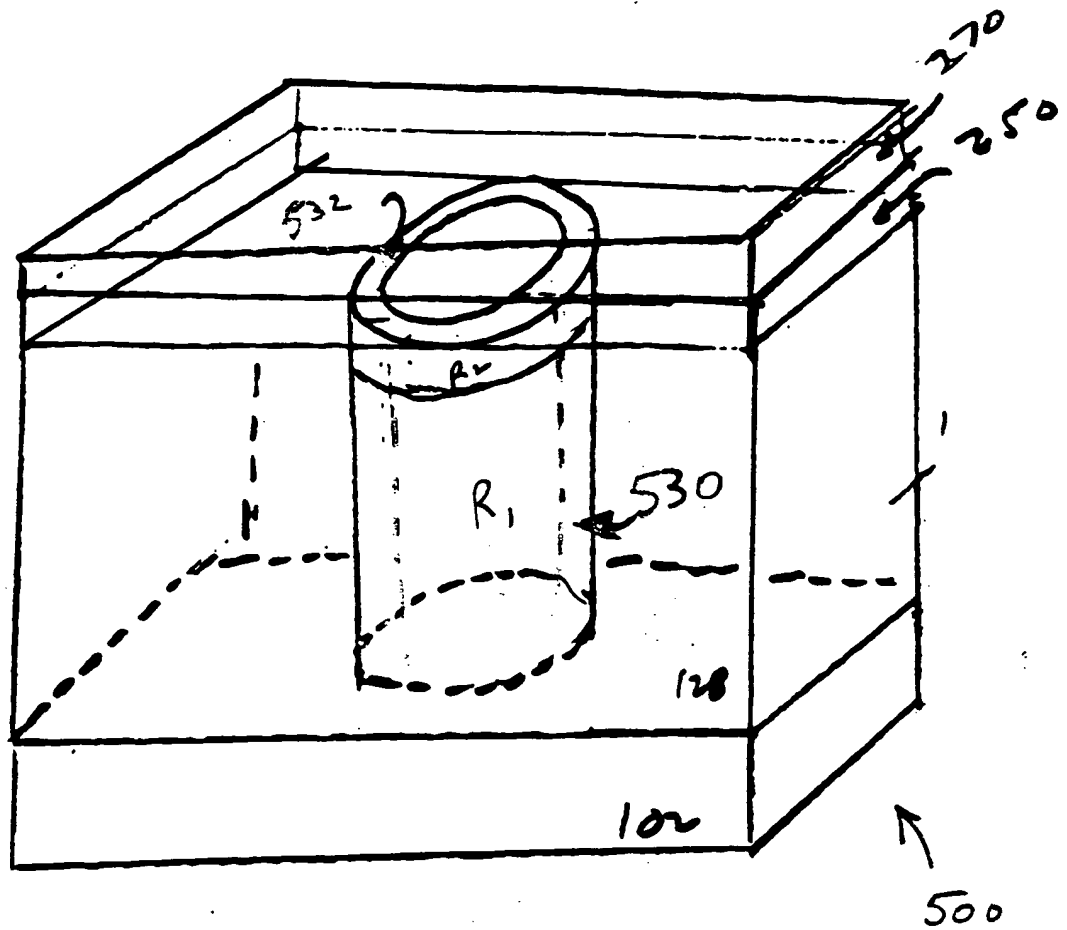


Figure 5A

09620313 07200

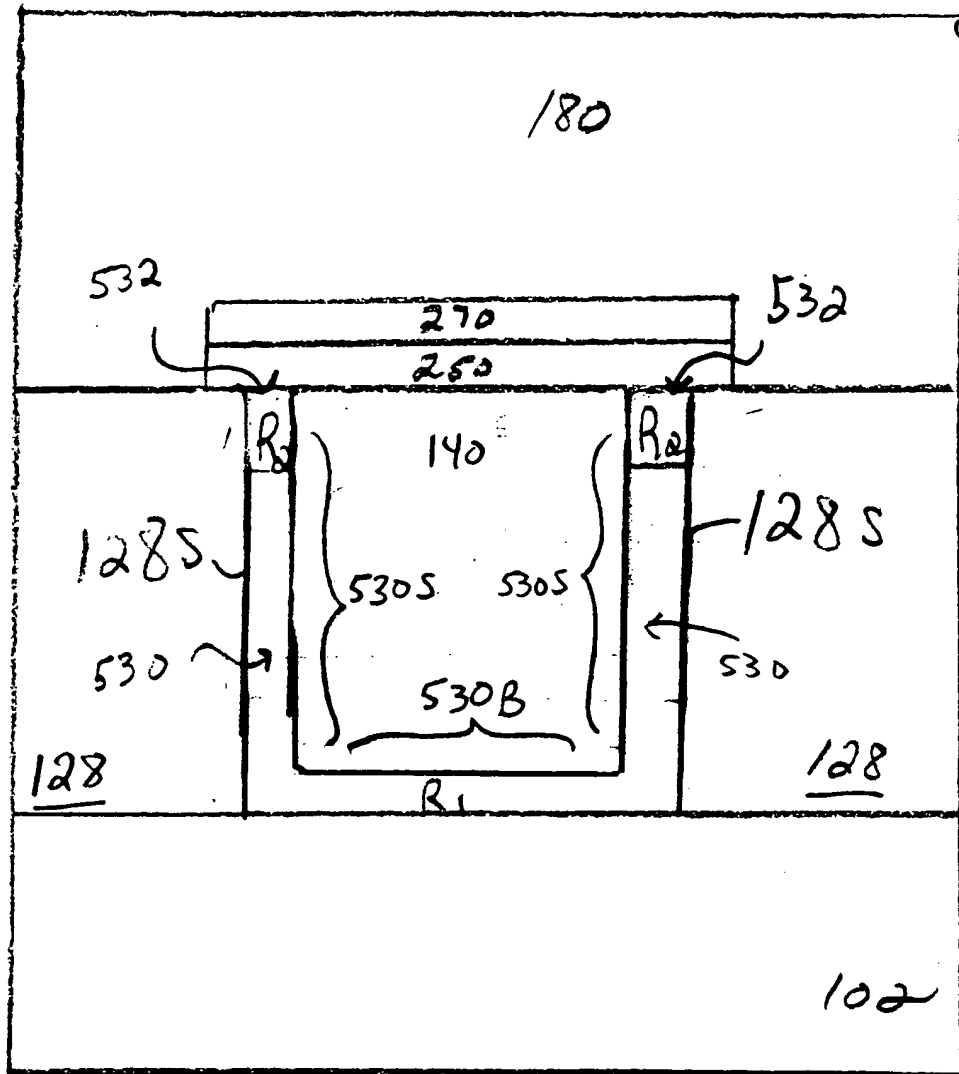


FIGURE 5B

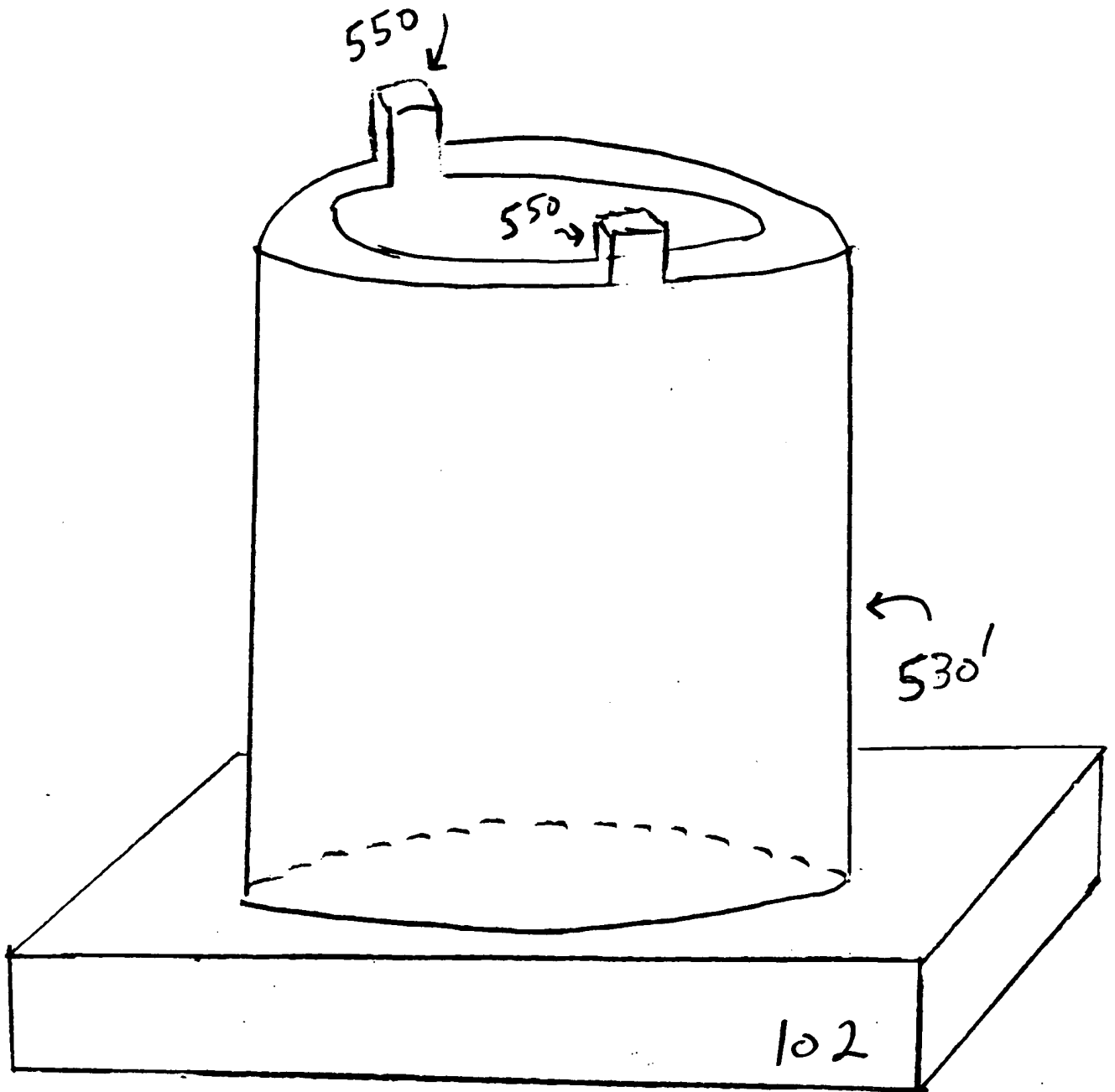
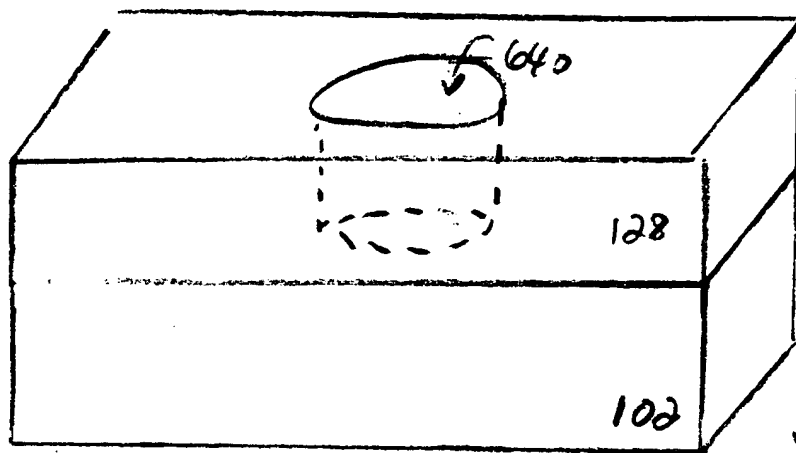
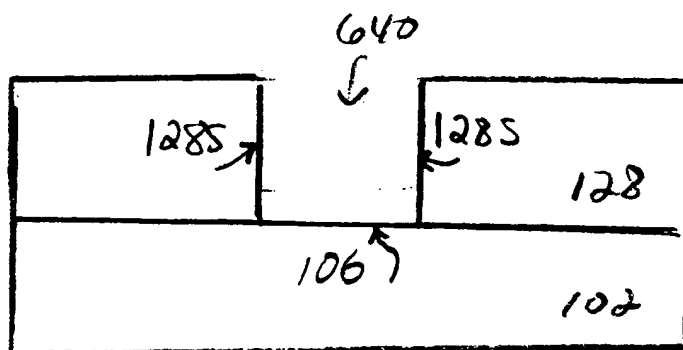


FIGURE 5C



6A

600A



6B

600A

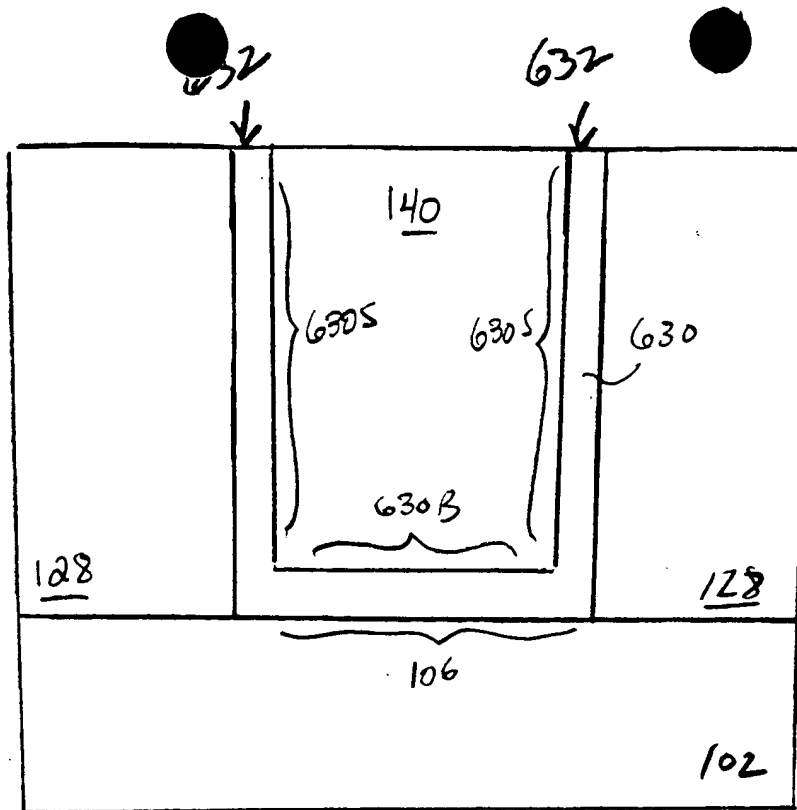
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Hand-drawn schematic diagram of a memory architecture. The diagram shows two main memory blocks, each labeled "633T" at the top and "128" at the bottom. An arrow labeled "640" points down to a central region between the two blocks. This central region contains a bracketed area labeled "633S" and "633B". The entire structure is labeled "106" at the bottom. A label "102" is located at the bottom right of the diagram.

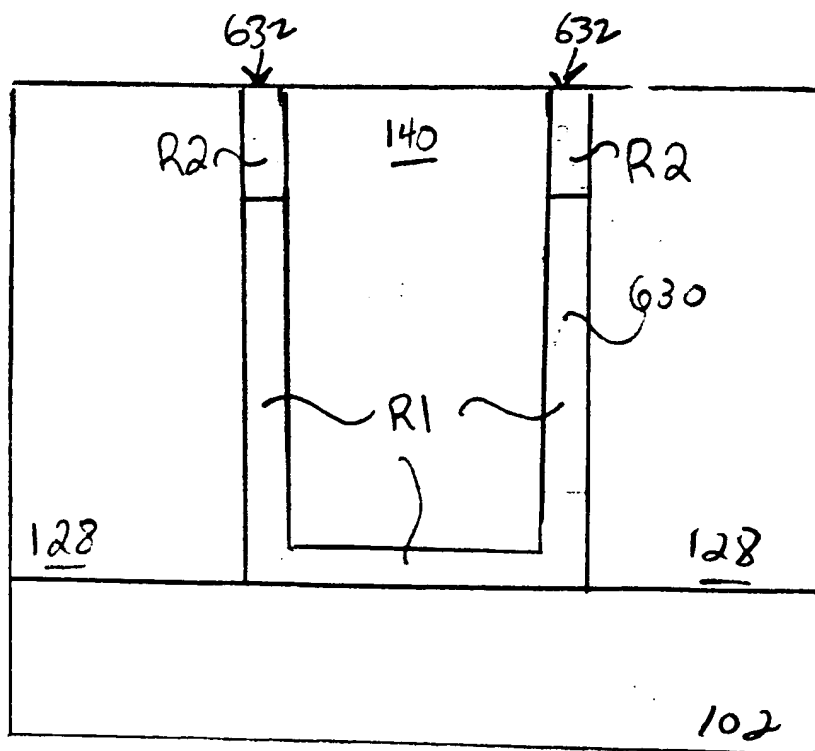
6c

A hand-drawn schematic diagram of a circuit layout. The diagram features two main rectangular blocks on the left and right, each labeled 633T at the top. Inside each block, there is a smaller rectangle labeled 128T with an upward-pointing arrow. To the left of the left block is a label 128. To the right of the right block is a label 128. Between the two main blocks is a central vertical section labeled 140 at the top. This section contains a bracketed area labeled 633S and 633B at the bottom. A label 633 is positioned to the left of this central section. At the bottom of the diagram, a horizontal line is labeled 106. The entire diagram is enclosed in a rectangular border.

GOOD



6E



6F

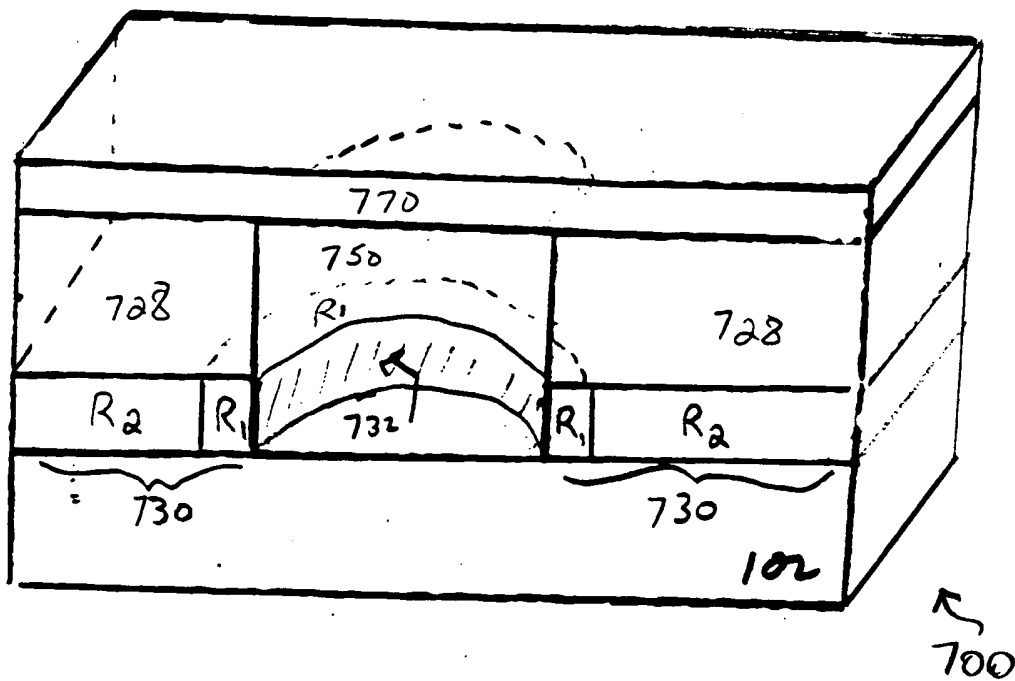


FIGURE 7A

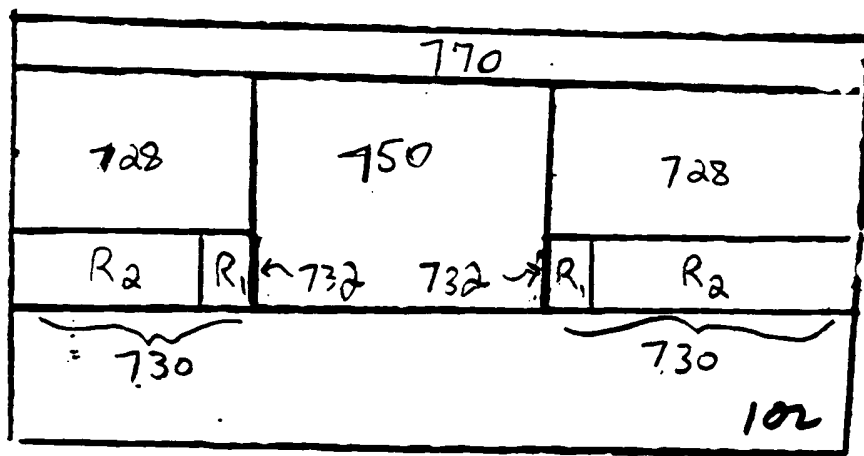


Figure 7B